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MAIL STOP PATENT APPLICATION

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

New U.S. Patent Application

Title: **SEMICONDUCTOR DEVICE MANUFACTURING METHOD**

Inventors and Addresses:

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Oita-shi, Japan

Sir:

We enclose the following papers for filing in the United States Patent and Trademark Office in connection with the above patent application.

1. Application - 40 pages, including 3 independent claims and 20 claims total.
2. Drawings - 5 sheets of formal drawings containing 20 figures.

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DUNNER LLP

3. Certified copy of Japanese Patent Application No. 2002-360230, filed on December 12, 2002.
4. Information Disclosure Statement and Information Disclosure Citation, PTO 1449 with documents attached.
5. The filing fee is calculated as follows:

Basic Application Filing Fee					\$770	\$ \$770.00
	Number of Claims		Basic	Extra Claims		
Total Claims	20	-	20	0	x \$18	\$
Independent Claims	3	-	3	0	x \$86	\$
<input type="checkbox"/> Presentation of Multiple Dep. Claim					+\$290	
Subtotal						\$ 770.00
Reduction by 1/2 if small entity						-
TOTAL APPLICATION FILING FEE						\$ 770.00

6. A check for \$770.00 is enclosed for filing fee.

This application is being filed under the provisions of 37 C.F.R. § 1.53(f). Applicants await notification from the Patent and Trademark Office of the time set for filing the Declaration.

Applicants claim the right to priority based on Japanese Patent Application No. 2002-360230, filed on December 12, 2002.

Please address all correspondence with respect to this application to:

**Finnegan, Henderson, Farabow,
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1300 I Street, N.W.
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Please accord this application an application number and filing date.

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The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. § 1.16 or §1.17 during the pendency of this application to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By: 

Richard V. Burgujian
Reg. No. 31,744

RVB/FPD/sci
Enclosures